This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A switch circuit comprising:

a first differential amplifier pair providing a portion of an isolation channel;

a second differential amplifier pair providing a portion of a transmit channel; and

a third differential amplifier pair providing a control bias for selecting either the transmit channel or the isolation channel, wherein the control bias maintains a substantially constant current density.

2. (Currently Amended) The switch circuit of claim 1, further comprising:

an input terminal coupled to the first differential amplifier pair and the second differential amplifier pair; and

an output terminal coupled to the second differential amplifier pair.

3. (Original) The switch circuit of claim 2, further comprising:

a control terminal coupled to the third differential amplifier pair.

4. (Original) The switch circuit of claim 3, wherein the control terminal provides a bias voltage to the third differential amplifier pair to enable one of two transistors within the differential amplifier pair.

5. (Original) The switch circuit of claim 1, wherein a first transistor of the third differential amplifier pair is disposed in the transmit channel, and a second transistor of the third differential amplifier pair is disposed in the isolation channel.

6. (Original) The switch circuit of claim 5, wherein enabling the first transistor permits an input signal to proceed to an output terminal of the circuit, and enabling the second transistor prohibits an input signal from proceeding to the output terminal.

7. (Currently Amended) The switch circuit of claim 1, wherein the circuit is formed as an integrated circuit on one of a Silicon Germanium, Silicon Gallium Arsenide or Indium Phosphide substrate.

8. (Original) The switch circuit of claim 1, wherein each of the first and second differential amplifier pairs comprise at least two transistors with their emitters coupled.

9. (Original) The switch circuit of claim 1, wherein the second differential amplifier pair comprises at least two transistors, wherein at least one inductor is coupled to each of the respective collectors of the at least two transistors.

10. (Currently Amended) The switch circuit of claim 1, wherein the substantially constant current density of the control bias is sufficient to enable a pulse width of the control bias for selecting either the transmit channel or the isolation channel to be ~~is~~ less than 500 picoseconds.

11. (Currently Amended) The switch circuit of claim 1, wherein the substantially constant current density of the control bias is sufficient to enable a pulse width of the control bias for selecting either the transmit channel or the isolation channel to be ~~is~~ between 200-300 picoseconds.

12. (Currently Amended) A method for providing isolation between the input and output of a circuit comprising the steps of:

providing a first channel including at least one first differential amplifier pair, said first channel providing isolation between the input and output of the circuit;

providing a second channel including at least one second differential amplifier pair, said second channel providing coupling between the input and output of the circuit; and providing a control bias which selects one of the first channel or the second channel, wherein said control bias maintains a substantially constant current density.

13. (Original) The method of claim 12, wherein the step of providing a control bias comprises supplying a control voltage to bases of a differential amplifier pair.

14. (Currently Amended) The method of claim 13, wherein the substantially constant current density of said control bias is sufficient to enable a pulse width of the control voltage is less than 500 picoseconds.

15. (Currently Amended) The method of claim 13, wherein the substantially constant current density of said control bias is sufficient to enable a pulse width of the control voltage for selecting one of said first channel or said second channel to be ~~is~~ between 200-300 picoseconds.

16. (new) The method of claim 12, wherein said first channel provides isolation between said signal input and said signal output over a 15 GHz to 26 GHz range.

17. (new) The method of claim 12, wherein said second channel provides gain between said signal input and said signal output over a 14 GHz to 28 GHz range.

18. (new) The method of claim 12, wherein said control bias is supplied by a DC current source.